Hall Ticket Number:

Code No. : 6211

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. I Year (ECE) II-Semester (Main) Examinations, July-2016

(Embedded Systems & VLSI Design)

Mixed Signal IC Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2=20 Marks)

1. Draw the resistor equivalence of a Switched capacitor and give the expression for resistance.
2. Describe Substrate Coupling in Mixed Signal IC Design.
3. What is the approach used in analyzing filters operating on signal frequency close to the clock frequency?
4. Mention the limitations of an Op-Amp based comparator.
5. Draw the circuit of a unity gain sampler for discrete time applications.
6. Explain how a Sample and Hold circuit can be generated using transmission gates.
7. Compare Nyquist rate and oversampling converters.
8. Describe the issues in designing Flash A/D converters.
9. Given that a 1-bit A/D converter has 6 dB SNR what sample rate is required using Oversampling without noise shaping to obtain a 96 dB SNR if f_o (signal frequency) = 25 KHz.
10. Give the linear model of type 1 PLL and draw its underdamped response to step input.

Part-B (5 × 10=50 Marks)

11. a) Explain how Analog and Digital circuits are implanted on the same substrate. What are the problems involved and how are they overcome? [6]

    b) Describe atleast two methods of realizing A/D conversion. [4]

12. a) What is a resettable gain circuit? Using Switched capacitors generate a capacitive reset gain circuit. [6]

    b) Suggest a latched comparator for high speed application. Discuss its design considerations. [4]

13. a) Consider the basic Sample and Hold circuit with C_{hld} = 1pF, C_{ox} = 1.92 pF/ $(\mu m)^2$ V_{th} = 0.8 V, (W/L) = 5 µm / 0.8 µm. Assume the power supply voltages are ± 25V and the input signal is 1 V Peak to Peak. Find the hold step for V_{in} = 1V and then repeat for V_{in} = -1 V to estimate the dc offset. [5]

    b) Explain the operation of a Bipolar track and Hold circuit. [5]

14. a) Mention the various types of binary scaled D/A Converters. Discuss the operation of a 4-bit R-2R based D/A converter with a neat diagram. [6]

    b) What is two step A/D conversion? Explain the operation of a two-step Nyquist rate A/D converter. [4]

Contd...2

15. a) Assuming Oversampling with no noise shaping find the approximate sampling rate required to obtain a maximum SNR of 80 dB on a signal with a 1 kHz bandwidth using a 1-bit quantizer. [4]

b) What is a delay locked loop? Explain its operation. [6]

16. a) A 0.5 mV signal must be resolved using a basic Op-Amp comparator whose output is 5 V. The Op-Amp unity gain frequency is 10 MHz. Find the maximum clocking rate of the comparator if reset and comparison phases are equal and if six time constants are allowed for settling. [5]

b) Explain how analog components are mimicked by digital operations. [5]

17. Answer any **two** of the following:

a) High input impedance Sample & Hold circuit [5]

b) Successive approximation A/D converter [5]

c) Applications of PLL [5]

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